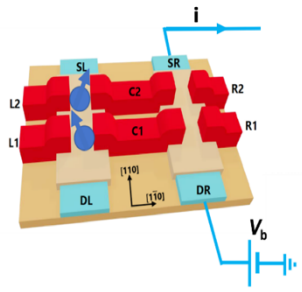
INSTITUT NEEL Grenoble

Post doc position in Si spin qubits– Academic year 2021-2022

Design and fabrication of spin qubit devices

Context : In quantum nanoelectronics, one of the major goals is the use of quantum mechanics for the development of nanoprocessors that are more and more efficient. This requires the ability to control quantum phenomena at the single electron scale within nanostructures. In this context, the degree of freedom of the electron spin has been identified as a potential candidate for the support of quantum information. We can define the elementary block of the nanoprocessor by capturing a single electron (and therefore its spin) inside a quantum dot. The development of a quantum circuit will follow the same methods of microelectronic circuits conception, by connecting the elementary bricks, while respecting the constraints of controlling the individual spins. Nowadays, in quantum dots systems, all the elementary operations required for the functioning of a quantum processor have been demonstrated in trapped spins of AsGa heterostructures. The effort of the spin qubits community turns to the transposition of these demonstrations for trapped spins in silicon structures, whose fabrication is compatible with CMOS industrial processes.



Example of a co-integrated device which could be develop during this project. It comprises three section. i) qubit part on the left nanowire contains two qubit (depicted with blue balls) and which are controlled using the gate L1 and L2. ii) the detector on the right nanowire, which is capacitively coupled to the qubits through C1 and C2. iii) The MRAM is serially connected with the detector. Therefore, the detector current output is sent to the MRAM to write the information.

Objectives and means available: The aim of this project is to develop the post fabrication process and characterization of silicon spin qubits using structures fabricated at the CEA-Leti. The interest is twofold: on one hand it permits a rapid characterization of the structures, on the other hand a way to quickly add new features to manipulate coherently the qubits (electron spin resonance antenna, micro-magnets, …) or to assist the readout (addition of local detectors and memories).

The candidate will benefit from the extensive knowledge of the Néel group in fabricating and characterizing devices with a full access to the clean room facility (ebeam lithography, deposition, etching) and the resources offered by the technical poles (electronics, cryogenics) for the electronic characterization.

Interactions and collaborations: This work is part of a large collaborative effort between the CEA-INAC, CEA-LETI and CNRS-Institut Néel to develop and push the technology of spin qubit in silicon and investigate its potential scalability. Therefore, the candidate will work in close collaboration with the LETI's device fabrication team to develop the structures dedicated to her/his project. Moreover, the applicant will benefit from the collaboration with Spintec on the integration of magnetic components in the CMOS device.

Skills and training: It is mandatory to have presented a PhD thesis defense in the following topics: condensed matter, micro–nanotechnologies or CMOS devices design/fabrication. It is essential to have good knowledge of semiconductor devices and an expertise in nanofabrication techniques (lithography, deposition etching, …) is highly desirable. A candidate familiar with device electrical characterization is a plus. Good written and spoken English skills are required, on the same way as communication, ability of writing reports/articles, and team work.

Foreseen start for the position: immediate
Salary : from 2050 to 2850 euros after tax, depending on experience
Duration : 24 months

Contacts: Matias Urdampilleta et Tristan Meunier
Institut Néel/ CNRS- Université Joseph Fourier
Matias.urdampilleta@neel.cnrs.fr
tristan.meunier@neel.cnrs.fr