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Metal oxide semiconductor structure using oxygen-terminated diamond

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Metal-oxide-semiconductor structures with aluminum oxide as insulator and p-type (100) mono-crystalline diamond as semiconductor have been fabricated and investigated by capacitance versus voltage and current versus voltage measurements. The aluminum oxide dielectric was deposited using low temperature atomic layer deposition on an oxygenated diamond surface. The capacitance voltage measurements demonstrate that accumulation, depletion, and deep depletion regimes can be controlled by the bias voltage, opening the route for diamond metal-oxide-semiconductor field effect transistor. A band diagram is proposed and discussed. © 2013 AIP Publishing LLC.

In order to overcome this problem, solutions based on two dimensional (2-D) hole gas are under investigation: (i) H-terminated diamond field effect transistor (FET) using hole accumulation layer.1–3 Such transistors demonstrate high frequency operation but deteriorate under high temperature conditions. (ii) Boron δ-FET consisting on a thin heavily doped (metallic) layer between two intrinsic layers resulting theoretically in high mobility (due to delocalisation of carrier away from ionized impurities induced by confinement). However, obtaining a very thin layer4 (<2 nm needed) is a technological challenge. Delta layers thinner than 2 nm are reported5 but did show neither quantum confinement nor enhancement of the mobility, which is yet too low for high frequency applications. (iii) Diamond/nitride heterojunctions FET6 has been recently proposed and their electronic properties are under investigation at this moment. Concerning more conventional semiconductor devices, the Si metal oxide semiconductor field effect transistor (MOSFET) is ubiquitous in digital and analog integrated electronic systems. The conducting or insulating behavior of the MOSFET is based on the electrostatic control of the band curvature at the oxide/semiconductor interface. Unfortunately, the physical properties of Si semiconductor do not allow to build efficient MOSFET for power electronics applications (generally insulated gate bipolar transistor is preferred but also limited to 4 kV). MOSFET based on other semiconductors, like III-V compounds or SiC, are progressing but the performances of such devices are not competitive with Si devices and anyway will be always lower than that expected for diamond based MOSFET.7 The main problem to fabricate a MOS structure is to achieve the semiconductor oxide interface with a sufficiently low interface states density. In that case, the different regimes of the MOS can be controlled: accumulation of majority carriers, depletion, deep depletion, or inversion of carrier (minority carrier density larger than majority carrier density at the interface). In most cases and contrary to the Si/Oxide interface, the too large density of interface states within the gap are charging under bias voltage, and the breakdown field of the oxide is reached before deep depletion or inversion regimes. Recent works reported investigation of Al2O3 deposited by Atomic Layer Deposition (ALD) on hydrogen-terminated diamond to stabilize8 or to study the band offset related to the hydrogen 2-D gas. MOS structures on diamond using high dielectric constant Ta2O5 oxides were also reported9 but did not show the deep depletion regime. In our case, in order to reach deep depletion or inversion regimes at the interface of Al2O3/diamond, we introduce an approach combining an oxygen-terminated diamond with low temperature ALD.12,13 Using this process, we demonstrate that such MOS capacitor can undergo accumulation, depletion, and deep depletion. The control of the interface regimes reported in this work opens the route for diamond MOSFET and more generally for diamond based electronics. This letter is organized as follows: the first part describes the experimental details and the diamond MOS fabrication using ALD technique for oxide deposition. In the second part, the capacitance measurements are detailed and analyzed in terms of control of the different regimes using the gate metal electrode.

The five structures investigated in this work consist of a stack of Al/Al2O3 gate electrode deposited on a boron-doped epitaxial diamond layer grown in a microwave plasma assisted chemical vapor deposition (MPCVD) reactor on Ib high pressure high temperature (HPHT) (100) diamond

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substrate. A schematic picture of the structure is shown in Fig. 1(a). Sample #0 is composed of a heavily doped diamond layer (named p++ and with boron concentration over the metal insulator transition) in order to fabricate Metal Insulator Metal (MIM) structure. The four other samples #1, #2, #3, and #4 are aimed to be MOS structures. They consist of B-doped diamond layers with a boron concentration of about few 10\(^{17}\) cm\(^{-3}\). The deposition was performed at 910°C with CH\(_4/H_2\) = 2% and B/C = 2 ppm. In sample #4, a heavily doped layer was grown between the substrate and p-layer with the same technique but with CH\(_4/H_2\) = 4%, B/C = 1200 ppm at 830°C. On each, an ohmic contact (Ti/Pt/Au annealed at 750°C under high vacuum) was evaporated directly on the epitaxial layer to act as reference contact (see Fig. 1(b)) for capacitance measurement.

Photolithography process was used in order to selectively deposit the dielectric oxide. Before that step, diamond surface oxygenation has been performed by two techniques: (i) for samples #0, #1, #3, #4 by deep UV ozone treatment and (ii) for sample #2 by oxygen RF plasma treatment.

Then, the 10 nm for sample #1 and 20 nm for #0, #2, #3, and #4 of Al\(_2\)O\(_3\) dielectric oxide have been deposited by ALD. In order to preserve the lithography resist, the ALD oxide has been deposited at low temperature (100°C). The ALD system used in the present experiments was Savannah 100 from Cambridge NanoTech. The precursor used was trimethylaluminum (TMA), and the oxidant was H\(_2\)O. Using the same window in resist, the dielectric has been covered by a 100 nm thick aluminum metal using electron beam evaporator. After resist removing, the electrical properties of the MOS capacitances have been measured using a Keithley 6517B source-electrometer apparatus for the static current/voltage I(V) characteristics and a Agilent E4980A Precision LCR Meter for the capacitance/voltage C(V) measurements. Frequency dependent capacitance measurements have been performed with a.c. signal frequency ranging from 100 Hz to 2 MHz and typical amplitude of 50 mV. Nyquist plots have been performed (i) to determine the series and parallel resistances of the stack and (ii) to find the most favorable frequency to measure the imaginary part of the total impedance (where the imaginary part/real part ratio is the highest) in order to determine more accurately the capacitance. The measurements reported in Fig. 2 were done with frequencies in the range of 50 kHz to 200 kHz.

Sample #0 is a MIM structure while the four other samples are MOS structures. In samples #1, #2, and #3, different oxide thicknesses and surface treatments were evaluated (see Table 1). In sample #3 (in regards of #1 and #2), the quality of the p-diamond layer has been improved, principally by reducing its thickness. Sample #4 is the same as #3 with an additional p++ buried layer in order to reduce the series resistance and simplify C(V) measurements and their interpretation. Thickness and doping of each sample are summarized in Table 1.

First of all, using the MIM structure of sample #0 made of a stack of metallic diamond, Al\(_2\)O\(_3\), and aluminum metal, the oxide properties were investigated. Al\(_2\)O\(_3\) oxide thickness value \(d_{ox}\) was measured by ellipsometry and found in good agreement with the targeted values reported in Table 1.

FIG. 1. (a) Schematic of the diamond metal oxide semiconductor structure and SEM image and (b) detailed stacks of each sample.

FIG. 2. (a) Capacitance \(C/C_{max}\) versus voltage measurement of the diamond MOS structures, (b) \(1/C^2\) versus voltage which enables us to determine the doping of diamond in case of deep depletion regime (samples #3 and #4) from the slope of the straight line for positive voltage, and (c) static current versus voltage of samples #1, #2, #3, and #4.
The capacitance was measured and found to be constant versus applied voltage (−10 V to 10 V) and versus frequency (100 Hz to 2 MHz). Due to the MIM structure, the resultant capacitance of this stack is equal to the oxide capacitance $C_{ox}$ given by

$$C_{ox} = \frac{\varepsilon_0 \varepsilon_{ox} S}{d_{ox}},$$

where $\varepsilon_0$ is the vacuum permittivity, $\varepsilon_{ox}$ is the relative permittivity of the oxide, and $S$ is the MOS capacitor area. The measured value of capacitance was 20% lower than the value expected if calculated with the $Al_2O_3$ relative permittivity given in literature for similar deposition process (i.e., low temperature ALD except the Si substrate).

In samples #1 and #2, different regimes can be observed on C(V) measurements (see Fig. 2(a)). For negative voltage ($V \leq -5$ V for #1 and $V \leq -3$ V for #2), the holes accumulation is observed. This regime is characterized by an almost flat capacitance theoretically equal to that of the oxide capacitance $C_{ox}$ (Eq. (1)) because the stack is like a planar capacitor (see Fig. 3(a)) composed of the oxide layer in between two electrodes (Al and diamond). But experimental capacitances in the accumulation regime take values above or below $C_{ox}$ according to the measurement frequency. A three elements circuit has been used to introduce the series resistance effect on the measurement. Indeed, in the ideal case, the capacitance is considered in parallel to the resistance of the conductor interface could be responsible of this electron generation mechanism to be observed. Minority carriers can be provided by thermal or optical generation of electron-hole pairs in the neutral part of the semiconductor but frequency of the a.c signal used to measured capacitance must be sufficiently low to be comparable to the inverse time constant related to the generation mechanism (approximate maximum value of $10^{-20}$ s$^{-1}$ for a mid gap trap level) in order that the charges could follow this a.c signal. In our case, no optical excitation was used and the frequency measurement is too high for thermal generation. Diamond p-layer of these two samples shows a large amount of defects such as hillocks (due to the large thickness of the layer), which are generally going through the whole depth of the layer. A mechanism providing electrons from neutral regions through these defects up to the oxide/diamond interface could be responsible of this electron generation. However, a measurement artifact due to the high

![FIG. 3. Band diagram of a theoretical diamond metal oxide at different applied bias voltages with an oxide thickness of 20 nm, a p-type diamond doped at $2.2 \times 10^{17}$ cm$^{-3}$, an affinity of O-terminated diamond of 1.7 eV, and an $Al_2O_3$ gap of 6.5 eV. The schematic band diagrams represent (a) the accumulation regime for $V = -5$ V, (b) the flat band regime for $V = -2.4$ V, (c) the depletion regime for $V = 0$ V, and (d) the inversion regime for $V = 7.5$ V. The inset in each band diagram shows the corresponding capacitance versus voltage measurements (inversion and deep depletion are both plotted).](image-url)
oxide leakage current or an impedance due to deep levels (as suggested above) cannot be discarded. In order to clarify this point, samples #3 and #4 were fabricated. Diamond layers are thinner, contain less defects, and in sample #4 a buried $p^{++}$ layer was added in order to reduce the series resistance and avoid measurement artifacts. For these two samples, the hole accumulation (with some frequency dispersion) and depletion are also observable like in samples #1 and #2, but instead of increasing again in the positive voltage range, the capacitance continues to decrease. This decrease is typical of the deep depletion regime. In fact, the $1/C^2$ versus voltage plot (see Fig. 2(b)) in this voltage range ($-2 \leq V \leq 10$ $V$) is linear and typical of the depletion of an homogeneous doped semiconductor over the depth. By applying a linear fit to this part, the effective doping of the $p$-diamond can be deduced from the slope for these two samples and are $3.6 \times 10^{17} \text{cm}^{-3}$ for sample #3 and $2.2 \times 10^{17} \text{cm}^{-3}$ for sample #4. These values are consistent with SIMS measurement performed on a similar sample where the boron doping level was measured between $2 \times 10^{17} \text{cm}^{-3}$ and $5 \times 10^{17} \text{cm}^{-3}$ over the whole depth of the layer (1.8 $\mu$m). The good agreement between $B$-density determined by $1/C^2$ and SIMS confirmed that the whole area of the MOS capacitor is active. Moreover, the observation of a deep depletion regime is consistent with the frequency range used for measurement.

Static I(V) measurements were also performed on these four MOS structures. Surprisingly for a stack containing an insulating layer, the current density is quite high as it can be seen in Fig. 2(c). Moreover, the I(V) characteristics of samples #1 and #2 are symmetrical while those of samples #3 and #4 are not with more current flowing in the negative voltage (holes accumulation) than in positive voltage (deep depletion). These observations could be related to the large range of the $\text{Al}_2\text{O}_3$ band gap values $E_{g}$ reported in literature: between $5.4 \text{eV}$ and $8.8 \text{eV}$. More precisely, $E_{g}=6.7\pm0.2\text{eV}$ (Refs. 19 and 23) for ALD deposited $\text{Al}_2\text{O}_3$ and even smaller if deposited by other techniques such as e-beam evaporation and spray pyrolysis method ($E_{g}=5.40-5.55\text{eV}$ (Ref. 20)). Diamond oxygenated surface electronic affinity is reported between $1.0\text{eV}$ and $1.7\text{eV}$ (Refs. 24–26). In Fig. 3, theoretical band diagrams are plotted at different applied voltages taking a band gap of $6.5\text{eV}$ for $\text{Al}_2\text{O}_3$, electronic affinity of $1.7\text{eV}$ for oxygenated diamond, and $2.2\times10^{17}\text{cm}^{-3}$ for $B$-doping. As shown, the barrier for holes is very low ($\approx0.4\text{eV}$) and could be inexistent if somewhat a smaller $\text{Al}_2\text{O}_3$ gap value or/and a little bit higher diamond affinity was considered. In that case, we expect a rectifier behavior with a high current limited by the diamond series resistance (and maybe also the contact resistance of the ohmic contact) for $V<0\text{V}$ and a blocking regime for $V>0\text{V}$ as observed for samples #3 and #4. Due to the much lower series resistance resulting from the $p++$ buried layer in sample #4, the current density in accumulation is higher in comparison to other samples. Moreover, for samples #3 and #4, the current is lower under positive voltage than under the negative ones. Assuming a very small barrier for holes (if any) when the structure is in deep depletion, the current is only limited by the insulating space charge region. On the contrary, for samples #1 and #2, the almost symmetrical current may be due to a parallel leakage path inside the depletion zone, as previously invoked to explain the capacitance anomalies.

Two different surface treatments (see Table I: DUV $\text{O}_3$ and $\text{O}_2$ plasma) to oxidize the diamond surface were tested. Samples #2 and #3 (different treatments with the same oxide deposition) show different behaviours, particularly in positive voltage. But as the crystalline quality of these two samples is different, no clear conclusion can be drawn about a possible influence of the surface treatment type.

The observation of a deep depletion regime in samples #3 and #4 opens the route for the fabrication of diamond MOSFET. In case of an n-MOSFET, the electrons needed to create inversion channel at the interface will be provided by n-type diamond boxes (source and drain). Such a transistor would be in off state because of a channel in depletion regime when no bias is applied to the gate (see band diagram in Fig. 3(c)), since the flat band voltage is not strongly negative ($V_{FB}\approx-2.4\text{V}$ in Fig. 3). This case is indeed achieved in samples #1, #2, and #3 as it can be seen on C(V) measurements in Fig. 2, while the more negative flat band voltage in sample #4, which might induce weak inversion, deserves future investigations. The on state (inversion) is expected to be reached for voltage larger than $V\approx2.5\text{V}$.

In this work, we demonstrated the fabrication of metal oxide diamond structures where different regimes are controlled by bias voltage: accumulation of holes, depletion, and deep depletion. The properties of the different samples have been discussed in order to compare the capacitance increase for positive applied voltages in two of the samples and the capacitance decrease induced by the deep depletion regime in two other ones. Electrical measurements enable us to investigate band offsets of the diamond MOS structures and show that even if no barrier exists for holes, a MOSFET using this stack would be operative since both off and on states could be reached.

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